Dynamic Runtime Assertions in Quantum Ternary Systems

Ehsan Faghih
North Carolina State University
Raleigh, USA
sfaghih@ncsu.edu

Huiyang Zhou
North Carolina State Uiversity
Raleigh, USA
hzhou@ncsu.edu

***Abstract*—With the rapid advancement of quantum computing technology, there is a growing need for new debugging tools for quantum programs. Recent research has highlighted the potential of assertions for debugging quantum programs. In this paper, we investigate assertions in quantum ternary systems, which are more challenging than those in quantum binary systems due to the complexity of ternary logic. We propose quantum ternary circuit designs to assert classical, entanglement, and superposition states, specifically geared toward debugging quantum ternary programs.**

***Index Terms*—Quantum computing, Quantum assertion, Quantum ternary circuit.**

I. Introduction

Quantum computing has distinctive advantages compared to classical computing, and the latest breakthroughs in quantum computer hardware have ignited optimistic prospects for unlocking the extraordinary potential of this field. Furthermore, it is shown that realizing quantum computing structures using multi-valued logic can bring many advantages over its binary counterpart [1], [2]. A careful examination of the product of the number's width (amount of digits) and the depth of digit (maximum number of symbols in each digit) as an influential factor of hardware cost in digital systems showed that the most economical radix is three. Quantum systems are no exception [3], [4]. Recent studies have shown that the design of quantum computers based on qutrit, the unit of quantum information in ternary representation, brings 37% more compactness than the quantum computer based on qubit, the unit of quantum information in binary representation [5], [6]. Quantum Ternary logic finds practical applications in the development of ternary computers such as quantum multiple-valued decision diagrams (QMDD) [7]. Ternary logic outperforms binary logic in several ways, one of which is its capacity to convey more information using fewer digits. This advantage enhances the flexibility for encoding and processing data. Additionally, it simplifies circuitry by reducing the necessity for numerous gates and connections, ultimately leading to reduced energy consumption [7]. It was also shown recently that quantum circuits via qutrits can introduce asymptotic improvements [8]. In quantum mechanics, ternary circuits can be physically realized with various technologies such as ion-trap [1].

The development of quantum computing systems at a large scale, enabling the execution of algorithms on extensive datasets, calls for better tools. Assertions are a primitive that can be used for both program debugging [9], [10] and error mitigation [11]. However, these prior works on quantum assertion were developed for quantum circuits with qubits. To further enhance the concept and leverage the benefits of quantum ternary logic, this paper focuses on supporting assertions in quantum circuits with ternary bits or qutrits.

The remainder of the paper is organized as follows. Section II provides background on quantum ternary gates and their operations and summarizes the prior works on quantum assertion. In Section III, we delve into our proposed designs for dynamic assertions in quantum ternary circuits, elaborating on their functioning. Section IV comprises an evaluation utilizing predefined test cases. Finally, Section V concludes.

II. Background

A. Quantum Ternary Logic

Quantum ternary-valued logic processors are a class of quantum systems in which each information unit, referred to as a qutrit, can be represented using three distinct 3×1 matrices. The states $|0\rangle$, $|1\rangle$, and $|2\rangle$ are considered the fundamental states, aka the computational basis states, of a qutrit, each possessing a distinctive representation as follows:

$$|0\rangle = \begin{bmatrix}1\\0\\0\end{bmatrix} \quad |1\rangle = \begin{bmatrix}0\\1\\0\end{bmatrix} \quad |2\rangle = \begin{bmatrix}0\\0\\1\end{bmatrix} \tag{1}$$

When considering complex numbers α, β, and γ, a qutrit can exist in a superposition state, simultaneously occupying a linear combination of the computational basis states $|0\rangle$, $|1\rangle$, and $|2\rangle$. This superposition state is denoted by $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle + \gamma|2\rangle$, where $|\alpha|^2 + |\beta|^2 + |\gamma|^2 = 1$. For an n-qutrit system, there are 3^n different computational basis states. For instance, in a two-qutrit system, the state can be represented as: $|\psi\rangle = \alpha_{00}|00\rangle + \alpha_{01}|01\rangle + \alpha_{02}|02\rangle + \alpha_{10}|10\rangle + \alpha_{11}|11\rangle + \alpha_{12}|12\rangle + \alpha_{20}|20\rangle + \alpha_{21}|21\rangle + \alpha_{22}|22\rangle$, where α is a complex coefficient, and $\sum_{\delta\in\{0,1,2\}^2}|\alpha|^2 = 1$.

There are six single-qutrit [Z] gates, and each of them is associated with a corresponding unitary 3×3 matrix, as illustrated below. Their functionalities are shown in Table 1.

$$Z(0) = \begin{bmatrix}1&0&0\\0&1&0\\0&0&1\end{bmatrix} \quad Z(+1) = \begin{bmatrix}0&0&1\\1&0&0\\0&1&0\end{bmatrix}$$

TABLE I
PERMUTATIONS OF 1-QUTRIT M-S GATES

PERMUTATIONS						
Input	Z(0)	Z(+1)	Z(+2)	Z(12)	Z(01)	Z(02)
0	0	1	2	0	1	2
1	1	2	0	2	0	1
2	2	0	1	1	2	0

$$Z(+2) = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{bmatrix} \quad Z(01) = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{bmatrix}$$

$$Z(02) = \begin{bmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \quad Z(12) = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{bmatrix}$$

In the context of qutrit systems, it is widely accepted that the quantum cost associated with single qutrit gates (like [Z] gates) and a controlled-[Z] gates is considered to be equal to unity [12] It is because, as far as our knowledge extends, there is currently no established benchmark for ternary quantum systems. In this study, we adopt the convention of assigning a quantum cost of unity to each M-S gate and Chrestenson gate.

Ternary Muthukrishnan-Stroud (M-S) Gates: A M-S gate consists of two types of primitive ternary quantum gates, namely 1-qutrit and 2-qutrit gates. Single-qutrit gates operate based on the Z transforms mentioned before, whereas two-qutrit gates include a control input for performing the Z transform, i.e., Controlled-[Z] gates. It means that only when the control qutrit is $|2\rangle$, the gate triggers the Z transformation on the target qutrit.

Chrestenson basis: Analogous to the Hadamard basis, i.e., $|+\rangle$ and $|-\rangle$ states, in qubit systems,

the Chrestenson basis [13] serves as a natural extension to the Hadamard basis in qutrit systems. There are two Chrestenson gates known as Ch1 and Ch2 which correspond to Hadamard gates in qubit systems. It is important to note that $Ch1Ch2 = I$ (identity matrix). Here, ω is the cube root of unity, i.e., $\omega^3 = 1$, and $1 + \omega + \omega^2 = 0$ [14].

$$|+\rangle = \frac{1}{\sqrt{3}}(|0\rangle + |1\rangle + |2\rangle)$$

$$|-_i\rangle = \frac{1}{\sqrt{3}}(|0\rangle + \omega^i|1\rangle + \omega^{2i}|2\rangle) \quad i \in \{1, 2\}$$

$$||_i\rangle = \frac{1}{\sqrt{3}}(|0\rangle + \omega^{2i}|1\rangle + \omega^i|2\rangle) \quad i \in \{1, 2\}$$

$$Ch1 = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \omega & \omega^2 \\ 1 & \omega^2 & \omega \end{bmatrix} \quad Ch2 = \begin{bmatrix} 1 & 1 & 1 \\ 1 & \omega^2 & \omega \\ 1 & \omega & \omega^2 \end{bmatrix}$$

B. Quantum Assertions

Huang et al. [15] proposed a statistical approach for quantum assertion. They identified three essential types of assertions for debugging quantum programs: classical assertions, superposition assertions, and entanglement assertions. Classical assertions involve checking quantum variables against classical values to determine if they match the desired values. Superposition assertions are used to verify whether a quantum variable is in a desired superposition state. Entanglement assertions focus on checking whether the entangled quantum variables exhibit the desired correlation. Statistical assertions require measurements of the qubits of interest, thereby being disruptive to program execution.

Liu et al. introduced the concept of dynamic quantum assertions [10], which means that the assertion check is performed during program execution and the program continues execution if there is no assertion error. In this paper, we introduce dynamic assertion circuits for classical, superposition, and entangled states in the context of ternary logic.

Liu et al. further proposed two systematic approaches for dynamic quantum state assertion, capable of asserting a broader range of quantum states, including pure and mixed states [16].

Li et al. introduced Proq, a runtime assertion scheme for quantum program testing and debugging [17]. Proq utilizes projections based on Birkhoff-von Neumann quantum logic, enabling efficient assertion verification through minimal measurements. Their work demonstrates the efficacy of projection-based assertions for bug detection and ensuring program semantics in both exact and approximate quantum programs.

Enabling runtime assertion in ternary quantum circuits shares similar challenges to those found in binary quantum computing and is demanding for two primary reasons. Firstly, the non-cloning theorem poses a fundamental limitation by prohibiting the exact replication of qubits, making conventional debugging and assertion checks challenging. Secondly, measuring a qubit results in the collapse of its superposition state into a classical state, leading to the loss of inherent parallel information. This unique challenge persists in the verification of assertions within quantum states. Additionally, in the context of ternary quantum circuits, there is a notable deficiency of strategies for error correction or bug detection. One potential reason is that the additional quantum state introduces more opportunities for errors. Designing robust error correction or detection systems that work effectively with ternary logic is an area of active research. Furthermore, designing and optimizing quantum gates for ternary logic is more complex compared to binary gates. Ternary gates, such as Toffoli gates with ternary inputs, have to account for three quantum states, making gate design and optimization more intricate [3].

III. QUANTUM TERNARY CIRCUITS FOR DYNAMIC ASSERTIONS

Our approach to enabling dynamic assertions revolves around the introduction of additional quantum bits, referred to as ancilla qutrits. These ancilla qutrits provide information about the qutrits under test. Instead of directly measuring the qutrits under test, we measure the ancilla qutrits. This allows us to verify assertions without disrupting the program

execution. However, it is crucial to ensure that measuring the ancilla qutrits does not impact the original quantum circuit. In the following sections, we outline our proposed circuits for each type of assertion.

To develop these assertion circuits, we first design two simple ternary circuits called A1 and A2 gates, depicted in Fig. 1.

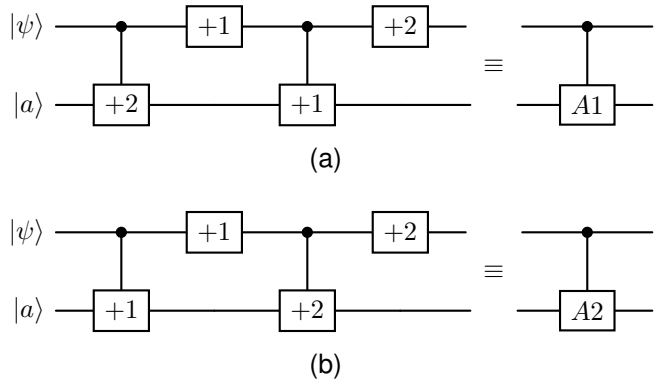

Fig. 1. The A1 and A2 circuits and their gate scheme symbol. $|a\rangle$ is an ancilla input.

An A1 gate adds its control qutrit value to its target qutrit. In the figure, the target is $|a\rangle$, and the control qutrit is $|\psi\rangle$. For example, if the control qutrit is set to 1 and the target is 0, the target would become 1 after A1, and the control qutrit remains the same. Similarly, A2 employs a similar principle to add (2 * controller value) to the target. Using the same example, if the controller is also set to 1, it will add 2 to its target. The gates A1 and A2 are formally defined as follows. Note that these gates become identity gates when the control bit is 0, and $i \in \{1, 2\}$.

$$\begin{cases} A1 : \text{if } (control = i) \text{ then target} = |target + i\rangle \ mod\ 3. \\ A2 : \text{if } (control = i) \text{ then target} = |target + 2i\rangle \ mod\ 3. \end{cases}$$

As shown in Fig. 1, the implementation of the gates involves the use of two 1-qutrit and two 2-qutrit gates. Consequently, the quantum cost of these operations is equal to 4, and their depth is also 4.

A. Dynamic Assertion for Ternary Classical Values

By asserting for ternary classical values, we aim to support $assert(|\psi\rangle == |i\rangle)$, where $|\psi\rangle$ is the qutrit of interest and $i \in \{0, 1, 2\}$. To achieve this, we propose the circuit depicted in Fig. 2. The circuit shown in Fig. 2 checks whether the state of $|\psi\rangle$ is equal to $|0\rangle$. The ancilla qutrit is initially set to $|0\rangle$ and is measured after the A1 gate operation. By initializing the ancilla qutrits to $|i\rangle$, the same circuit can be used to assert ($|\psi\rangle$ ==$|2i \ mod\ 3\rangle$).

Proof. Let us consider the case where the ancilla input is set to $|0\rangle$, and we are asserting whether $|\psi\rangle$ is equal to $|0\rangle$. If $|\psi\rangle$ is in a classical state, taking values of either $|0\rangle$, $|1\rangle$, or $|2\rangle$, the resulting states of the $|\psi_0\rangle$ can be represented as $|00\rangle$, $|10\rangle$, or $|20\rangle$. Therefore, the resulting states, denoted as $|\psi_1\rangle$, would be $|00\rangle$, $|11\rangle$, or $|22\rangle$, respectively. Consequently,

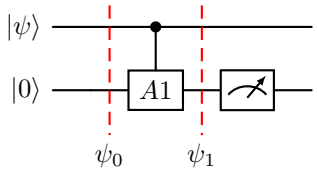

Fig. 2. Circuit for classical-value assertion, assert($|\psi\rangle$ == $|0\rangle$).

when the ancilla qutrit is measured and yields the state $|0\rangle$, it signifies that $|\psi\rangle$ must be $|0\rangle$, indicating no assertion error. If the measurement outcome is $|1\rangle$, it implies that $|\psi\rangle$ must be $|1\rangle$, and if it is $|2\rangle$, $|\psi\rangle$ must be $|2\rangle$, indicating an assertion error.

If the $|\psi\rangle$ is in a superposition state, represented as $|\psi\rangle$ = a$|0\rangle$ + b$|1\rangle$ + c$|2\rangle$ due to a bug or runtime error, the resulting $|\psi_0\rangle$ becomes a$|00\rangle$ + b$|10\rangle$ + c$|20\rangle$ and $|\psi_1\rangle$ becomes a$|00\rangle$ + b$|11\rangle$ + c$|22\rangle$, indicating an entangled state. This entanglement leads to a unique behavior during the measurement of the ancilla qutrit. If the measurement outcome is $|0\rangle$ (no assertion error), the qutrit under test is projected into the classical state $|0\rangle$, denoted as $|\psi'\rangle$ = $|0\rangle$. Conversely, if the measurement outcome is $|1\rangle$ (an assertion error), it is projected into the classical state $|1\rangle$. In the context of an assertion check ($|\psi\rangle$ == $|0\rangle$), the proposed circuit has the potential to automatically correct the qutrit if it is in a superposition state, resulting in no assertion error. However, if the qutrit cannot be corrected into the expected classical state, an assertion error occurs. The probability of obtaining a measurement result of $|0\rangle$, $|1\rangle$ or $|2\rangle$ is determined by the squared magnitudes of coefficients $|a|^2$, $|b|^2$ and $|c|^2$, respectively. The probability distribution of assertion errors over multiple runs can be used to estimate a, b, and c, as needed.

The cases when the ancilla qutrit is set to $|1\rangle$ and $|2\rangle$ can be derived similarly to assert for $|2\rangle$ and $|1\rangle$, respectively.

B. Dynamic Assertion for Entangled States

We propose dedicated circuits to check whether two qutrits under test are in certain entangled states. Fig 3 shows the two groups of commonly used entangled states, and we propose two circuits as shown in Fig 4 to assert them, respectively.

a$|00\rangle$ + b$|12\rangle$ + c$|21\rangle$	a$|00\rangle$ + b$|11\rangle$ + c$|22\rangle$
a$|01\rangle$ + b$|10\rangle$ + c$|22\rangle$	a$|02\rangle$ + b$|10\rangle$ + c$|21\rangle$
a$|02\rangle$ + b$|11\rangle$ + c$|20\rangle$	a$|01\rangle$ + b$|12\rangle$ + c$|20\rangle$
(a)	(b)

Fig. 3. Two entangled groups of ternary states

In Fig. 4, circuit (a) is designed for asserting entangled states in group (a) of Fig. 3. By setting the ancilla qutrits to different initial states, this circuit verifies whether the qutrit of interest $|\psi_0\rangle$ is in one of the entangled states listed in group (a). Next, we explain the assertion process for asserting the ternary state a$|00\rangle$ + b$|12\rangle$ + c$|21\rangle$, when the ancilla bit is set to $|0\rangle$).

Proof. $|\psi_0\rangle$ = a$|000\rangle$ + b$|120\rangle$ + c$|210\rangle$
$|\psi_1\rangle$ = a$|000\rangle$ + b$|121\rangle$ + c$|212\rangle$

$|\psi_2\rangle$ = a$|000\rangle$ + b$|120\rangle$ + c$|210\rangle$ = $|\psi\rangle \otimes |0\rangle$

$|\psi\rangle \otimes |0\rangle$ is the ternary entangled state that we intended to assert, along with an un-entangled ancilla qutrit. By measuring the ancilla bit, we can determine if we have successfully achieved the desired state without collapsing the entangled state. If the measurement yields a zero, it indicates that the system is in the correct state and the entanglement is preserved.

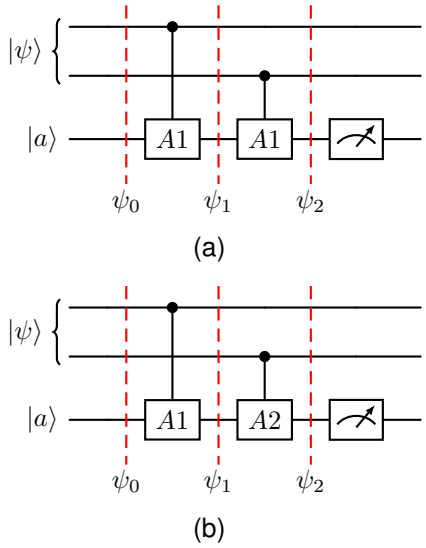

Fig. 4. Two proposed circuits to assert ternary entanglement. (a) Proposed circuit to assert the entangled state in group *a* of Fig 3. (b) Proposed circuit to assert the entangled state in group *b* of Fig 3.

If the input qutrits are not entangled in the expected state, it can be expressed as $|\psi\rangle$ = a$|00\rangle$+ d$|01\rangle$+ g$|02\rangle$+ e$|10\rangle$+ h$|11\rangle$+ b$|12\rangle$+ i$|20\rangle$+ c$|21\rangle$+ f$|22\rangle$. Then, the circuit produces the following states:

$$|\psi_0\rangle = [a\,|000\rangle + d\,|010\rangle + g\,|020\rangle + e\,|100\rangle + h\,|110\rangle + b\,|120\rangle + i\,|200\rangle + c\,|210\rangle + f\,|220\rangle].$$
$$|\psi_1\rangle = [a\,|000\rangle + d\,|010\rangle + g\,|020\rangle + e\,|101\rangle + h\,|111\rangle + b\,|121\rangle + i\,|202\rangle + c\,|212\rangle + f\,|222\rangle].$$
$$|\psi_2\rangle = [a\,|000\rangle + d\,|011\rangle + g\,|022\rangle + e\,|101\rangle + h\,|112\rangle + b\,|120\rangle + i\,|202\rangle + c\,|210\rangle + f\,|221\rangle].$$

TABLE II
TERNARY CIRCUIT OUTPUTS BASED ON CORRESPONDING ANCILLA AND $|\psi\rangle$ STATES, REFERRING TO FIG. 4. AND FIG. 3.

Circuit	$\|\psi\rangle$	Ancilla value	Output
Fig.4b	$a\,\|00\rangle + b\,\|11\rangle + c\,\|22\rangle$	$\|0\rangle$	$\|\psi\rangle \otimes \|0\rangle$
	$a\,\|02\rangle + b\,\|10\rangle + c\,\|21\rangle$	$\|2\rangle$	$\|\psi\rangle \otimes \|0\rangle$
	$a\,\|01\rangle + b\,\|12\rangle + c\,\|20\rangle$	$\|1\rangle$	$\|\psi\rangle \otimes \|0\rangle$
Fig.4a	$a\,\|00\rangle + b\,\|12\rangle + c\,\|21\rangle$	$\|0\rangle$	$\|\psi\rangle \otimes \|0\rangle$
	$a\,\|01\rangle + b\,\|10\rangle + c\,\|22\rangle$	$\|2\rangle$	$\|\psi\rangle \otimes \|0\rangle$
	$a\,\|02\rangle + b\,\|11\rangle + c\,\|20\rangle$	$\|1\rangle$	$\|\psi\rangle \otimes \|0\rangle$

When measuring the ancilla qutrit, the result can be either $|0\rangle$, $|1\rangle$ or $|2\rangle$. If the result is $|0\rangle$, the state $|\psi_2\rangle$ is projected to a$|000\rangle$ + b$|120\rangle$ + c$|210\rangle$ = (a$|00\rangle$ + b$|12\rangle$ + c$|21\rangle$) $\otimes$ $|0\rangle$, forcing the input qutrits into an entangled state. Likewise, if the result is $|1\rangle$ or $|2\rangle$, the state $|\psi_2\rangle$ is projected to the $(d\,|011\rangle + e\,|101\rangle + f\,|221\rangle)$ or $(g\,|022\rangle + h\,|112\rangle + i\,|202\rangle)$ terms, respectively representing different entangled states. In these cases, an assertion error would be reported as the measurement result is not 0. The probability of measuring $|0\rangle$, $|1\rangle$ or $|2\rangle$ can be used to compute the coefficients *a* to *i*, if needed.

Following similar steps, we can see that by initializing the ancilla qutrits to $|1\rangle$ or $|2\rangle$, the same circuit can be employed to assert whether the state $|\psi\rangle$ is equal to a$|02\rangle$ + b$|11\rangle$ + c$|20\rangle$ or a$|01\rangle$ + b$|10\rangle$ + c$|22\rangle$ respectively. This allows for the reuse of the circuit with different initializations of the ancilla qutrits to verify different desired states.

The same proof can also be applied to assert the entangled states within the group *b*. Table II lists the states to be asserted along with the proper ancilla qutrit settings and the circuit to be used.

C. Dynamic Assertion for Superposition

In binary quantum computing, a common pattern is to use Hadamard gates to put input qubits into an equal/uniform superposition state, denoted as $|+\rangle = \frac{1}{\sqrt{2}}(|0\rangle + |1\rangle)$. As mentioned earlier, in ternary quantum computing, Ch1 and Ch2 gates, which operate based on the Chrestenson basis, serve a similar purpose. To verify such uniform superposition states, including $|+\rangle$, $|-_1\rangle$ or $|-_2\rangle$, we propose a circuit as shown in Fig. 5.

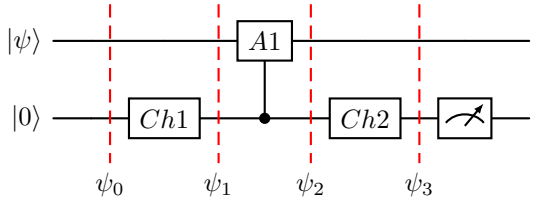

Fig. 5. Circuit for asserting equal superposition.

Proof. As shown in Fig 5, if $|\psi\rangle$ is equal to $|+\rangle$ and the ancilla is initialized to $|0\rangle$, the circuit produces the following states:

$$|\psi_0\rangle = a\,|00\rangle + b\,|10\rangle + c\,|20\rangle\,,\ (a = b = c = \tfrac{1}{\sqrt{3}})$$
$$|\psi_1\rangle = \tfrac{1}{3}[|0\rangle \otimes (|0\rangle + |1\rangle + |2\rangle) + |1\rangle \otimes (|0\rangle + |1\rangle + |2\rangle) + |2\rangle \otimes (|0\rangle + |1\rangle + |2\rangle)]$$
$$= \tfrac{1}{3}[(|00\rangle + |01\rangle + |02\rangle) + (|10\rangle + |11\rangle + |12\rangle) + (|20\rangle + |21\rangle + |22\rangle)]$$
$$|\psi_2\rangle = \tfrac{1}{3}[|00\rangle + |11\rangle + |22\rangle + |10\rangle + |21\rangle + |02\rangle + |20\rangle + |01\rangle + |12\rangle]$$

$$
\begin{aligned}
|\psi_3\rangle = \tfrac{1}{3\sqrt{3}}[&|00\rangle + |01\rangle + |02\rangle + |10\rangle + \omega^2|11\rangle + \omega|12\rangle + |20\rangle \\
&+ \omega|21\rangle + \omega^2|22\rangle + |10\rangle + |11\rangle + |12\rangle + |20\rangle \\
&+ \omega^2|21\rangle + \omega|22\rangle + |00\rangle + \omega|01\rangle + \omega^2|02\rangle \\
&+ |20\rangle + |21\rangle + |22\rangle + |00\rangle + \omega^2|01\rangle + \omega|02\rangle + |10\rangle \\
&+ \omega|11\rangle + \omega^2|12\rangle] \\
&=> \\
|\psi_3\rangle = \tfrac{3}{3\sqrt{3}}[&|00\rangle + |10\rangle + |20\rangle] = |+\rangle \otimes |0\rangle
\end{aligned}
$$

Given that $(\omega^3 = 1)$ and $(\omega^2 + \omega + 1 = 0)$, and if the qutrit is in the uniform superposition state, denoted as $|\psi\rangle = |+\rangle$, then the coefficients a, b and c are equal to $1/\sqrt{3}$. In this case, $|\psi_2\rangle$ would be as described in the above-mentioned Proof. The expression of $|\psi_2\rangle$ clearly indicates that the two qutrits in the circuit are entangled. To resolve this entanglement, an additional $Ch2$ gate is included at the end of the circuit. Consequently, the state $|\psi_3\rangle$ will be equal to $\frac{1}{\sqrt{3}}[|00\rangle + |10\rangle + |20\rangle] = |+\rangle \otimes |0\rangle$. We can follow the same process to assert for other uniform superposition states as shown in Table III.

TABLE III
OUTPUT ANALYSIS OF THE CIRCUIT IN FIG. 5 FOR VARIOUS ANCILLA AND $|\psi\rangle$ STATES.

$\|\psi\rangle$	Ancilla value	Output
$\|+\rangle$	$\|0\rangle$	$\|+\rangle \otimes \|0\rangle$
$\|+\rangle$	$\|1\rangle$	$\|+\rangle \otimes \|1\rangle$
$\|+\rangle$	$\|2\rangle$	$\|+\rangle \otimes \|2\rangle$
$\|-_1\rangle$	$\|0\rangle$	$\|-_1\rangle \otimes \|2\rangle$
$\|-_1\rangle$	$\|1\rangle$	$\|-_1\rangle \otimes \|0\rangle$
$\|-_1\rangle$	$\|2\rangle$	$\|-_1\rangle \otimes \|1\rangle$
$\|-_2\rangle$	$\|0\rangle$	$\|-_2\rangle \otimes \|1\rangle$
$\|-_2\rangle$	$\|1\rangle$	$\|-_2\rangle \otimes \|2\rangle$
$\|-_2\rangle$	$\|2\rangle$	$\|-_2\rangle \otimes \|0\rangle$

As listed in Table III, various uniform superposition states can be asserted using the circuit presented in Fig 5. For instance, if the expected state is $|\psi\rangle = |-_1\rangle$, then the ancilla qutrit needs to set to $|1\rangle$. In this configuration, the ancilla qutrit measurement result of 0 indicates the absence of an assertion error, while a different measurement outcome suggests otherwise.

IV. EVALUATION

In this section, we present various use cases to assess the efficacy of our proposed assertion circuits.

A. Asserting Classical States

We commenced by testing a ternary quantum half-adder (HA) circuit from the prior work [6]. Our objective is to validate the final results through sample inputs. Let us consider a specific scenario where the input states are set as $|AB\rangle = |22\rangle$. As a result, the expected output should be $|SC\rangle = |11\rangle$ with an overflow occurred since the carry-out (Cout) should be equal to one. In this case, we select our assertion circuit and set $|2\rangle$ as its ancilla input to $assert(carryout == |1\rangle)$. Upon measuring the outcome of the ancilla qutrit, when the Cout is $|1\rangle$, we obtain $|0\rangle$ without disturbing the original HA circuit. However, should the Cout have a value of $|0\rangle$ or $|2\rangle$, it indicates that the overflow is incorrect. This leads to an assertion error, as the ancilla qutrit is no longer $|0\rangle$.

To illustrate the process of debugging the HA circuit, let's hypothetically consider a scenario where a bug was introduced during the design phase. For instance, let's assume that a [+1] gate was mistakenly used before the controlled-[+2] gate as the initial gate in the HA circuit (as illustrated in Fig.6). Despite this discrepancy, the initial values remain consistent for both $|AB\rangle$ and the two additional qutrits. However, it is important to note that since the Cout qutrit should be checked

it must be the qutrit that controls the [A1] gate. After integrating the suggested assertion circuit with an ancilla state of $|2\rangle$, an error becomes evident upon measuring the fourth qutrit (the bottom-most qutrit). In this case, an undesired outcome would arise for the Cout. Instead of the intended value of 1, it would be 2. Consequently, with the proposed classical assertion circuit to detect a value of 1, the measurement outcome would yield a non-zero result, leading to an assertion error.

Given that the quantum cost of utilizing each MS gate is one unit, the quantum cost (QC) of the classical assertion circuit is calculated to be 4. The depth of the classical assertion circuit would be 4, reflecting the number of logical levels within the circuit.

B. Asserting Superposition States

To illustrate the use of the proposed circuit in asserting ternary superposition states, we conducted a test using a reference circuit designed to produce the expected superposition state $\frac{1}{\sqrt{3}}[|0\rangle + \omega|1\rangle + \omega^2|2\rangle]$. This state is the result of applying a [Ch1] gate to the input value $|1\rangle$. In a hypothetical scenario, we inadvertently employed a [Ch2] gate instead of a [Ch1] gate while starting with an initial input state of $|1\rangle$, as shown in Fig.7, which led to the creation of a hypothetical bug. As a result, we obtained $\frac{1}{\sqrt{3}}[|0\rangle + \omega^2|1\rangle + \omega|2\rangle]$ instead of the expected state. By using the superposition assertion circuit, we detected this discrepancy, confirming it as an assertion error. According to the Table III, as the expected state is $|-_1\rangle$, the ancilla qutrit is initialized to be $|1\rangle$.

proof. According to Fig 7, if $|\psi\rangle$ is equal to $|1\rangle$, the circuit produces the following states as a result of the mentioned bug:

$$
\begin{aligned}
|\psi_0\rangle &= \tfrac{1}{\sqrt{3}}[|01\rangle + \omega^2|11\rangle + \omega|21\rangle] \\
|\psi_1\rangle &= \tfrac{1}{3}[|0\rangle \otimes (|0\rangle + \omega|1\rangle + \omega^2|2\rangle) + \omega^2|1\rangle \otimes (|0\rangle + \omega|1\rangle \\
&\quad + \omega^2|2\rangle) + \omega|2\rangle \otimes (|0\rangle + \omega|1\rangle + \omega^2|2\rangle)] \\
&= \tfrac{1}{3}[(|00\rangle + \omega|01\rangle + \omega^2|02\rangle) + (\omega^2|10\rangle + |11\rangle + \omega|12\rangle) \\
&\quad + (\omega|20\rangle + \omega^2|21\rangle + |22\rangle)]
\end{aligned}
$$

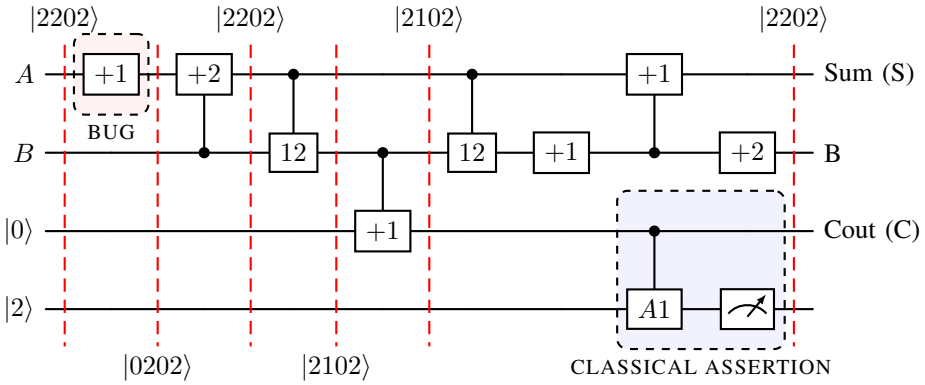

Fig. 6. Classical assertion in a half adder circuit for $|1\rangle$ using the proposed circuit in Fig. 2 with ancilla qutrit being $|2\rangle$. The functionality of the gates, e.g., the '*12*' gate, is shown in TableI. Here, a non-zero output will be measured because of the bug, leading to an assertion error (There is no overflow, though it is expected).

$$|\psi_2\rangle = \tfrac{1}{3}[|00\rangle + \omega\,|11\rangle + \omega^2\,|22\rangle + \omega^2\,|10\rangle + |21\rangle + \omega\,|02\rangle + \omega\,|20\rangle + \omega^2\,|01\rangle + |12\rangle]$$

$$|\psi_3\rangle = \tfrac{1}{3\sqrt{3}}[|00\rangle + |01\rangle + |02\rangle + \omega\,|10\rangle + |11\rangle + \omega^2\,|12\rangle + \omega^2\,|20\rangle + |21\rangle + \omega\,|22\rangle + \omega^2\,|10\rangle + \omega^2\,|11\rangle + \omega^2\,|12\rangle + |20\rangle + \omega^2\,|21\rangle + \omega\,|22\rangle + \omega\,|00\rangle + \omega^2\,|01\rangle + |02\rangle + \omega\,|20\rangle + \omega\,|21\rangle + \omega\,|22\rangle + \omega^2\,|00\rangle + \omega\,|01\rangle + |02\rangle + |10\rangle + \omega\,|11\rangle + \omega^2\,|12\rangle]$$

$$=>$$

$$|\psi_3\rangle = \tfrac{3}{3\sqrt{3}}[|02\rangle + \omega^2\,|12\rangle + \omega\,|22\rangle] = |-_2\rangle \otimes |2\rangle$$

As it can be seen, we did not obtain a $|0\rangle$ as our output for the second qutrit, which is essential for confirming the correctness of the final result. Since a value other than $|0\rangle$ is measured (in this case, $|2\rangle$), an assertion error is reported.

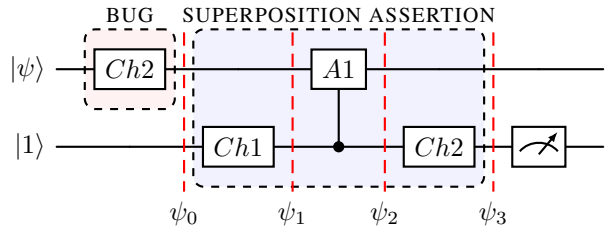

Fig. 7. Checking the uniform superposition generation using the assertion circuit in Fig. 5 with ancilla qubit being $|1\rangle$.

C. Asserting for Entangled States

To showcase the efficacy of our proposed circuit for asserting a ternary entangled state, we apply it to another circuit presented in reference [18] for generating entangled states. The circuit is shown in Fig. 8. We aim to ascertain the accuracy of the circuit's output and detect any potential bugs. Let us consider a scenario where the input state has changed because a [+1] gate is added mistakenly on the second qutrit. $|\alpha\beta\rangle$ is set to $|00\rangle$. In this specific case, the expected output from the circuit should be a$|00\rangle$ + b$|11\rangle$ + c$|22\rangle$, where $a = b = c = \frac{1}{\sqrt{3}}$. To ensure the accuracy of the result, we employ our proposed assertion circuit for checking the expected entangled state. Based on the anticipated output $\frac{1}{\sqrt{3}}(|00\rangle + |11\rangle + |22\rangle)$, we find that the appropriate circuit for asserting the target state, which belongs to group *b* in Fig.3, is the second circuit in Fig.4(*b*) with the ancilla = $|0\rangle$ as shown in Fig.8. In the case that the circuit's outcome aligns with the predetermined expected state, the measured value will be $|0\rangle$. Otherwise, deviations from the expected state will yield measured values of $|1\rangle$ or $|2\rangle$, both signifying the occurrence of an assertion error. With the abovementioned bug, i.e., the erroneous application of a [+1] gate on the first qutrit, a non-zero value will be measured for the second qutrit, resulting in an assertion error.

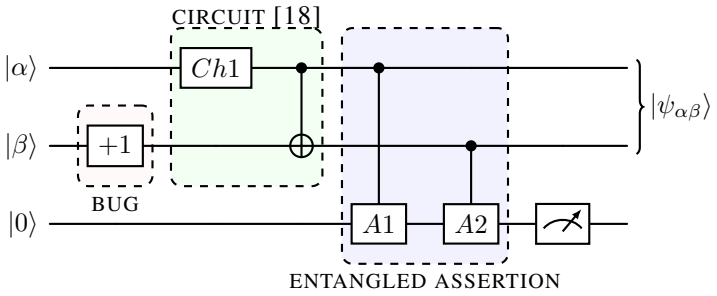

Fig. 8. Checking entangled qutrits introduced in [18] using the proposed assertion circuit in Fig. 4b to detect the bug. The entangled circuit with ancilla qutrit being $|0\rangle$ asserts for $\frac{1}{\sqrt{3}}(|00\rangle + |11\rangle + |22\rangle)$.

However, our assertion circuit for checking entangled states can only detect changes in classical values and is unable to identify variations in phase characteristics. For instance, the assertion circuit cannot distinguish among $\frac{1}{\sqrt{3}}(|00\rangle+|11\rangle+|22\rangle)$ and $\frac{1}{\sqrt{3}}(|00\rangle+\omega\,|11\rangle+\omega^2\,|22\rangle)$ and $\frac{1}{\sqrt{3}}(|00\rangle+\omega^2\,|11\rangle+\omega\,|22\rangle)$ states. To remedy this limitation, we propose to employ both the superposition assertion circuit and the entangled assertion circuit, as depicted in Fig. 9. This way, all the qutrit states listed in Table IV can be asserted. For example, suppose the anticipated entangled state is $\frac{1}{\sqrt{3}}(|00\rangle+|11\rangle+|22\rangle)$. However, when utilizing the original circuit [18] with the considered bug, i.e., a [+1] gate on the first qutrit before the [Ch1] gate on the

same qutrit, the output will be $\frac{1}{\sqrt{3}}(|00\rangle + \omega\,|11\rangle + \omega^2\,|22\rangle)$, with distinct phases. In order to discern this distinction, we added our proposed superposition assertion circuit, denoted as the SA block. Because the [Ch1] gate's output will not be $\frac{1}{\sqrt{3}}(|00\rangle + |11\rangle + |22\rangle)$ with the same phases, the [SA] circuit alters the state of the fourth ancilla qutrit, resulting in a state other than $|0\rangle$ (here, $|2\rangle$). Hence, even though the entangled asserting circuit, which found no errors, keeps its initial input intact, the third and fourth ancilla qutrits' outputs will be in the $|01\rangle$ state because [SA] found an asserting error. Given that $|00\rangle$ is the sole correct assertion, any output other than $|00\rangle$ for the last two qutrits is categorized as an assertion error. To assert and debug the other scenarios, only the ancilla qutrits in Fig. 9. need to be adjusted according to the expected stated. This information is provided in both Table II and Table III. The quantum cost of the merged technique is 14. The evaluation information is summarized in Table V. With this table, one can determine the logical delay and quantum cost associated with the use of each quantum ternary asserting circuit.

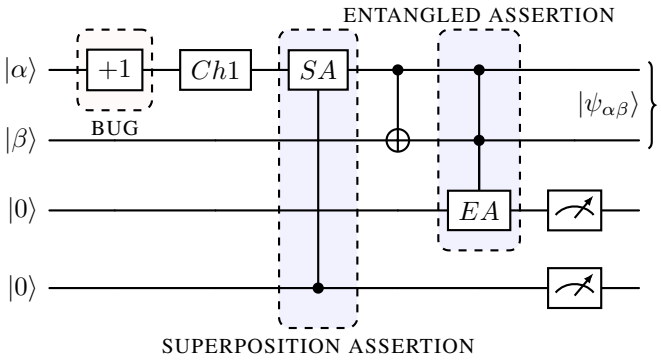

Fig. 9. Asserting entangled qutrits introduced in [18] using the proposed combined assertion circuits to detect phase errors. The assertion circuit with ancilla qutrits equal to $|00\rangle$ asserts for $\frac{1}{\sqrt{3}}(|00\rangle + |11\rangle + |22\rangle)$. The [SA] circuit is the proposed superposition assertion in Fig. 5, and the [EA] circuit is the proposed entanglement assertion in Fig. 4b.

TABLE IV
TABLE OF THE TEST CASE CIRCUIT RESULTS AND THE ANCILLA QUTRITS INITIALIZING FOR ASSERTING THEM BASED ON FIG. 9. (FOURTH QUTRIT IS THE BOTTOM-MOST)

		Measurement Output	
Input $\|\alpha\beta\rangle$ [18]	Output of circuit [18]	Third qutrit	Fourth qutrit
$\|00\rangle$	$\frac{1}{\sqrt{3}}(\|00\rangle + \|11\rangle + \|22\rangle)$	0	0
$\|01\rangle$	$\frac{1}{\sqrt{3}}(\|01\rangle + \|12\rangle + \|20\rangle)$	1	0
$\|02\rangle$	$\frac{1}{\sqrt{3}}(\|02\rangle + \|10\rangle + \|21\rangle)$	2	0
$\|10\rangle$	$\frac{1}{\sqrt{3}}(\|00\rangle + \omega\,\|11\rangle + \omega^2\,\|22\rangle)$	0	2
$\|11\rangle$	$\frac{1}{\sqrt{3}}(\|01\rangle + \omega\,\|12\rangle + \omega^2\,\|20\rangle)$	1	2
$\|12\rangle$	$\frac{1}{\sqrt{3}}(\|02\rangle + \omega\,\|10\rangle + \omega^2\,\|21\rangle)$	2	2
$\|20\rangle$	$\frac{1}{\sqrt{3}}(\|00\rangle + \omega^2\,\|11\rangle + \omega\,\|22\rangle)$	0	1
$\|21\rangle$	$\frac{1}{\sqrt{3}}(\|01\rangle + \omega^2\,\|12\rangle + \omega\,\|20\rangle)$	1	1
$\|22\rangle$	$\frac{1}{\sqrt{3}}(\|02\rangle + \omega^2\,\|10\rangle + \omega\,\|21\rangle)$	2	1

TABLE V
EVALUATION SUMMARY FOR EACH QUANTUM TERNARY ASSERTING CIRCUIT

Proposed Circuit	Cost	Delay
Fig. 2.	4	4
Fig. 4.	8	7
Fig. 5.	6	6
Fig. 9.	8+6	7+6

V. CONCLUSION

This paper presents our proposed circuits for assertions in quantum ternary circuits. The supported assertions include classical states, a set of entangled states, and uniform superposition states. With our proposed designs, we show that it is feasible to support dynamic assertions in quantum ternary logic, although they may be more conceptually complex than their binary counterpart. We then provide use cases to show how such assertions can be used to capture bugs in ternary quantum logic.

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